FAIRCHILD SEMICONDUCTOR®

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FIN1108 — LVDS 8-Port, High-Speed Repeater

Features

- Greater than 800Mbps Data Rate
- 3.3V Power Supply Operation
- 3.5ps Maximum Random Jitter and 135ps Maximum Deterministic Jitter
- Wide Rail-to-rail Common Mode Range
- LVDS Receiver Inputs Accept LVPECL, HSTL, and SSTL-2 Directly
- Ultra-low Power Consumption
- 20ps Typical Channel-to-channel Skew
- Power-off Protection
- 7.5kV HBM ESD Protection
- Meets or Exceeds the TIA/EIA-644-A LVDS Standard
- 48-Lead TSSOP Package
- Open-circuit Fail-safe Protection
- V_{BB} Reference Output

Descriptions

This eight-port repeater is designed for high-speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology.

The FIN1108 accepts and outputs LVDS levels with a typical differential output swing of 330mV, which provides low EMI at ultra-low power dissipation even at high frequencies. The FIN1108 provides a V_{BB} reference for AC coupling on the inputs. In addition, the FIN1108 can directly accept LVPECL, HSTL, and SSTL-2 for translation to LVDS.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FIN1108MTD	-40 to +85°C	48-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide	Tube
FIN1108MTDX	-40 to +85°C	48-Lead, Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Pin Configuration

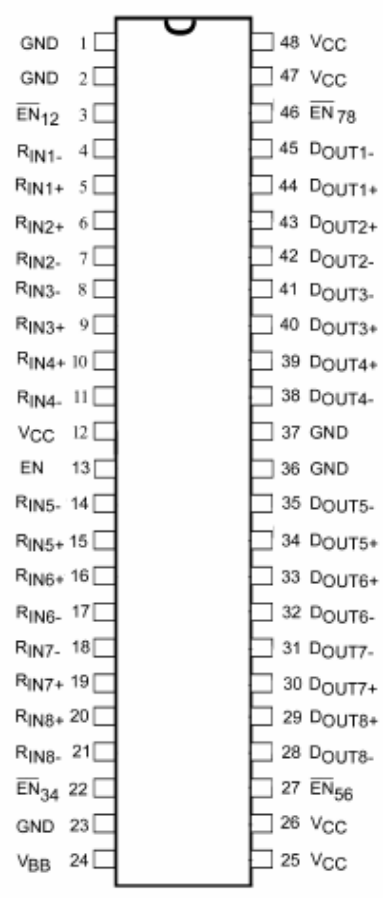


Figure 1. Pin Configuration

Pin Definitions

Pin #	Name	Description
1,2,23,37,36	GND	Ground.
3	$/EN_{12}$	Inverting driver enable for D_{OUT1} and D_{OUT2}.
4,7,8,11,14,17,18,21	R_{IN1-},R_{IN2-},R_{IN3-},$R_{IN5-}$$R_{IN6-}$,$R_{IN7-}$,$R_{IN8-}$	Inverting LVDS input.
5,6,9,10,15,16,19,20	R_{IN1+},R_{IN2+},R_{IN3+},$R_{IN5+}$$R_{IN6+}$,$R_{IN7+}$,$R_{IN8+}$	Non-inverting LVDS input.
12,25,26,47,48	VCC	Power supply pin.
13	EN	Driver enable for all outputs.
22	$/EN_{34}$	Inverting driver enable for D_{OUT3} and D_{OUT4}.
24	V_{BB}	Reference voltage output.
27	$/EN_{56}$	Inverting driver enable for D_{OUT5} and D_{OUT6}.
28,31,32,35,38,41,42,45	D_{OUT8-},D_{OUT7-},D_{OUT6-},$D_{OUT5-}$$D_{OUT4-}$,D_{OUT3-},D_{OUT2-},D_{OUT1-}	Inverting drive output.
29,30,33,34,39,40,43,44	D_{OUT8+},D_{OUT7+},D_{OUT6+},$D_{OUT5+}$$D_{OUT4+}$, D_{OUT3+},D_{OUT2+},D_{OUT1+}	Non-inverting drive output.
46	$/EN_{78}$	Inverting driver enable for D_{OUT7} and D_{OUT8}.

Functional Diagram

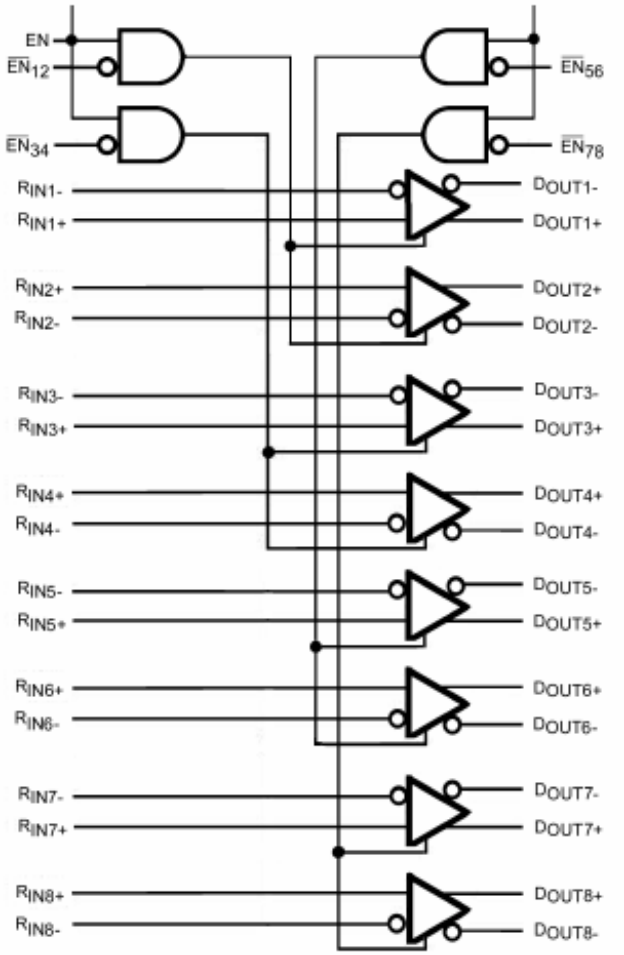


Figure 2. Functional Diagram

Table 1. Function Table

Inputs				Outputs	
EN	$/EN_{XX}$	D_{IN+}	D_{IN-}	D_{OUT+}	D_{OUT-}
HIGH	LOW	HIGH	LOW	HIGH	LOW
HIGH	LOW	LOW	HIGH	LOW	HIGH
HIGH	LOW	Fail-Safe		HIGH	LOW
Don't Care	HIGH	Don't Care	Don't Care	High Impedance	High Impedance
LOW	Don't Care	Don't Care	Don't Care	High Impedance	High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+4.6	V
V_{IN}	LVDS DC Input Voltage	-0.5	+4.6	V
V_{OUT}	LVDS DC Output Voltage	-0.5	+4.6	V
I_{OSD}	Driver Short-Circuit Current	Continuous	10	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature, Soldering, 10 seconds		+260	°C
ESD	Human Body Model, JESD22-A114		7500	V
	Machine Model, JEDEC: JESD22-A115		400	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
$\|V_{ID}\|$	Magnitude of Differential Voltage	100	mV to V_{CC}	V
V_{IC}	Common Mode Voltage Range	$(0V + \|V_{ID}\|/2)$	$(V_{CC} - \|V_{ID}\|/2)$	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

Typical values are at T_A=25°C with V_{CC}=3.3V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input Threshold HIGH	V_{IC}=+0.05V, + 1.2V, or V_{CC} - 0.05V Figure 3			100	mV
V_{TL}	Differential Input Threshold LOW	V_{IC}=+0.05V, + 1.2V, or V_{CC} - 0.05V Figure 3	-100			mV
V_{IH}	Input HIGH Voltage (EN or /EN)		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (EN or /EN)		GND		0.8	V
V_{OD}	Output Differential Voltage	R_L=100Ω, Driver Enabled, Figure 4	250	330	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.230	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OS}	Short-Circuit Output Current	D_{OUT+}=0V and D_{OUT-}=0V, Driver Enabled		-3.4	-6.0	mA
		V_{OD}=0V, Driver Enabled		±3.4	±6.0	mA
I_{IN}	Input Current (EN, /EN, D_{INx+}, D_{INx-})	V_{IN}=0V to V_{CC}, Other Input=V_{CC} or 0V for Differential Input			±20	µA
I_{OFF}	Power-off Input or Output Current	V_{CC}=0V, V_{IN} or V_{OUT}=0V to 3.6V			±20	µA
I_{CCZ}	Disabled Power Supply Current	Drivers Disabled			20	mA
I_{CC}	Power Supply Current	Drivers Enabled, Any Valid Input Condition			80	mA
I_{OZ}	Disabled Output Leakage Current	Driver Disabled, D_{OUT+}=0V, to 3.6V or D_{OUT-}=0V to 3.6V			±20	µA
V_{IC}	Common Mode Voltage Range		V_{ID}/2		V_{CC}-(V_{ID}/2)	V
C_{IN}	Input Capacitance	Enable Input		3		pF
		LVDS Input		3		
C_{OUT}	Output Capacitance			3		pF
V_{BB}	Output Reference Voltage	V_{CC}=3.3V, I_{BB}=0 to -275µA	1.125	1.200	1.375	V
R_T	Terminating Resistance			100		Ω

AC Electrical Characteristics

Typical values are at T_A=25°C with V_{CC}=3.3V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PLHD}	Differential Output Propagation Delay LOW-to-HIGH	R_L=100Ω, C_L=5pF V_{ID}=200mV to 450mV, V_{IC}= V_{ID}/2 to V_{CC} – (V_{ID}/2) Duty Cycle=50% Figure 3	0.75	1.10	1.75	ns
t_{PHLD}	Differential Output Propagation Delay HIGH-to-LOW		0.75	1.10	1.75	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.29	0.40	0.58	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.29	0.40	0.58	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$			0.02	0.20	ns
$t_{SK(LH)}$	Channel-to-Channel Skew[1]			0.02	0.15	ns
$t_{SK(HL)}$				0.02	0.15	
$t_{SK(PP)}$	Part-to-Part Skew[2]				0.5	ns
f_{MAX}	Maximum Frequency[3][4]		400	>630		MHz
t_{PZHD}	Differential Output Enable Time from Z to HIGH	R_L=100Ω, C_L=5pF Figure 4, Figure 5		3.0	5.0	ns
t_{PZLD}	Differential Output Enable Time from Z to LOW			3.1	5.0	ns
t_{PHZD}	Differential Output Disable Time from HIGH to Z			2.2	5.0	ns
t_{PLZD}	Differential Output Disable Time from LOW to Z			2.5	5.0	ns
t_{DJ}	LVDS Data Jitter, Deterministic	V_{ID}=300mV, PRBS=2^{23}-1, V_{IC}=1.2V at 800Mbps		80	135	ps
t_{RJ}	LVDS Clock Jitter, Random (RMS)	V_{ID}=300mV V_{IC}=1.2V at 400Mbps		1.9	3.5	ps

Notes:

1. $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.
2. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.
3. Passing criteria for maximum frequency is the output V_{OD} >250mV and the duty cycle is better than 45% / 55% with all channels switching.
4. Output loading is transmission-line environment only; C_L is <1pF of stray test fixture capacitance.

Test Diagrams

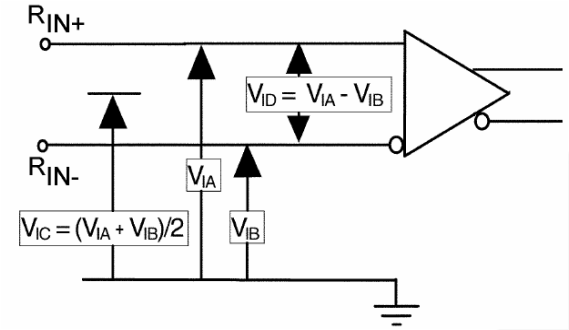


Figure 3. Differential Receiver Voltage Definitions

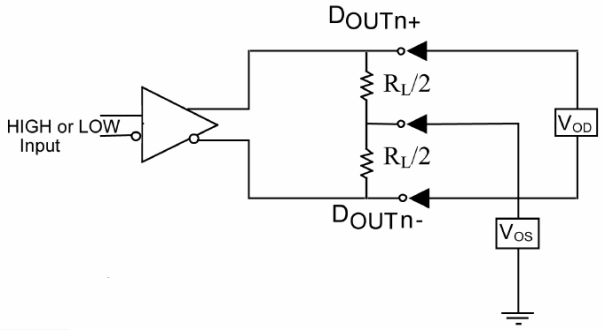
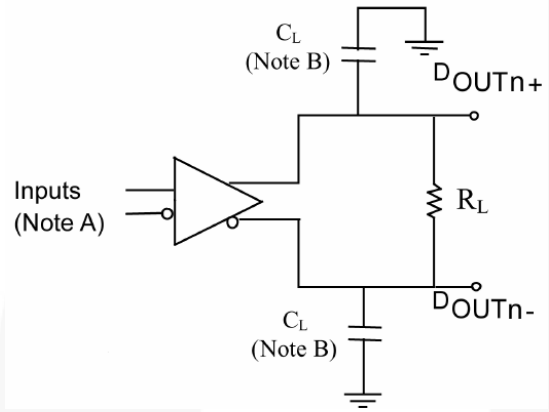


Figure 4. Differential Driver DC Test Circuit



Notes: All LVDS input pulses have
frequency=10MHz, t_R or t_F<0.5ns.
C_L includes all probe and jig capacitance.

Figure 5. Differential Driver Propagation Delay and Transition Time Test Circuit

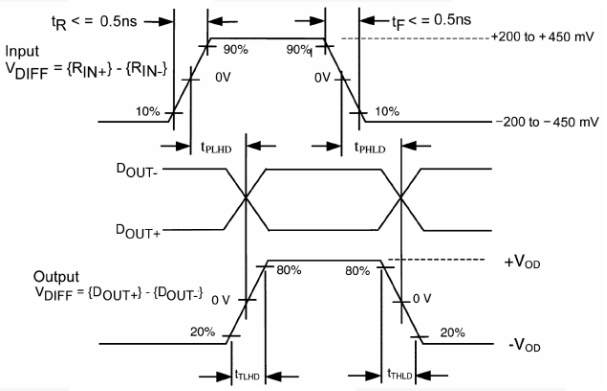
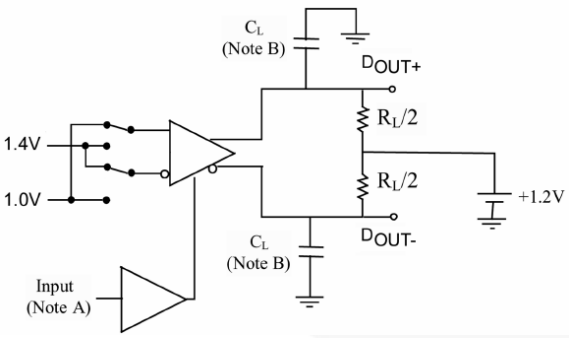


Figure 6. AC Waveform



Notes: All LVTTL input pulses have
frequency=10MHz, t_R or t_F<2ns.
C_L includes all probe and jig capacitance.

Figure 7. Differential Driver Enable and Disable Circuit

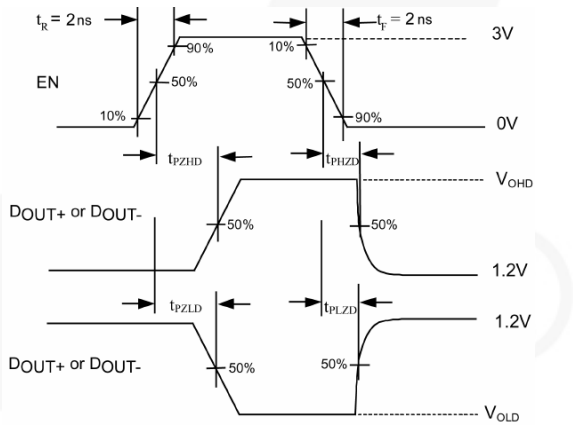


Figure 8. Enable and Disable AC Waveforms

Physical Dimensions

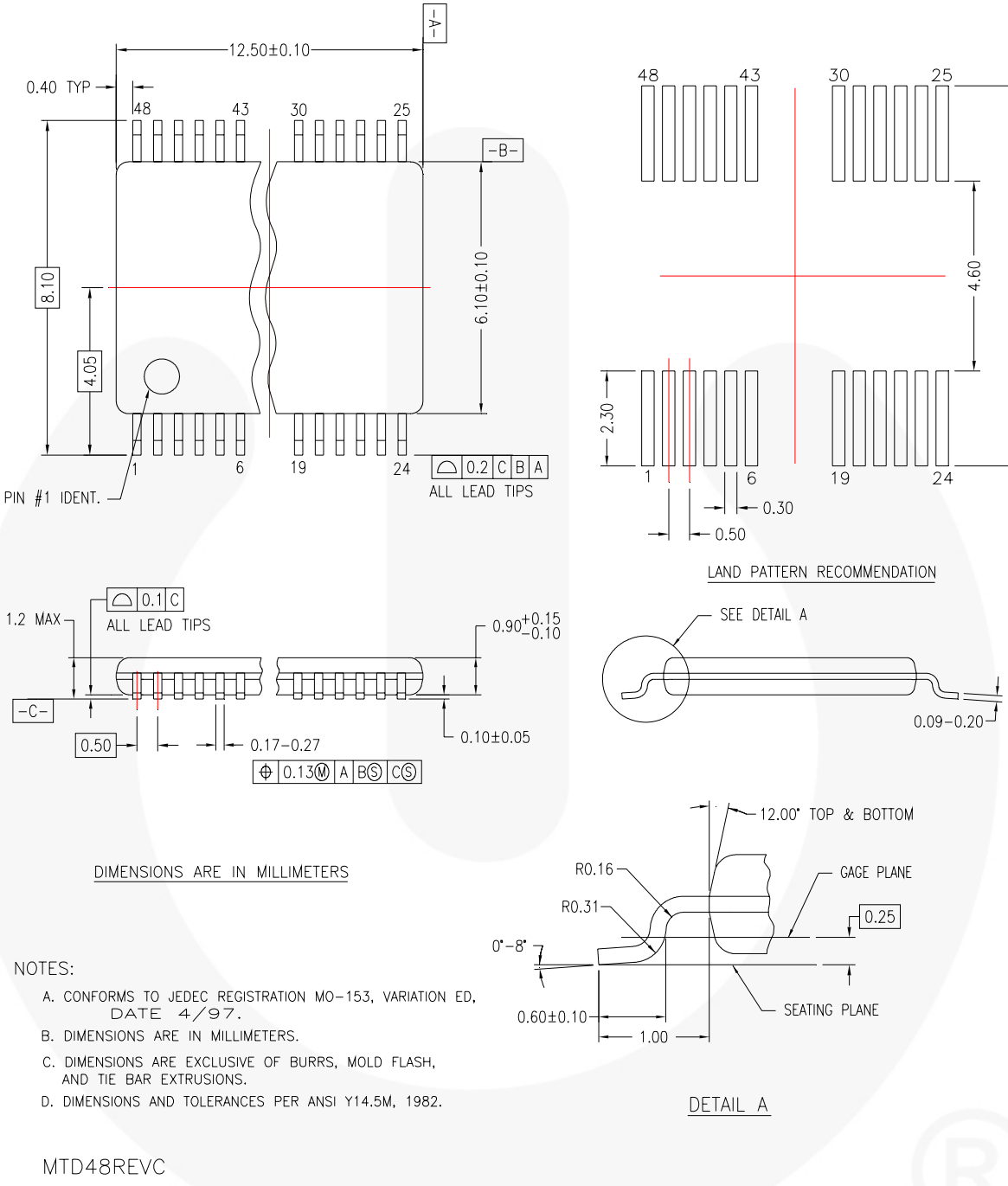


Figure 9. 48-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

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